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EXAMINER	
CRAIG, DWIN M	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/475,262	Applicant(s) ROBERTS, BEN D.	
	Examiner Dwin M Craig	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-63 have been presented for reconsideration in light of Applicant's Request for Continued Examination (RCE) under 37 C.F.R. 1.1114.

Response to Arguments

2. Applicant's arguments filed on 11-23-2003 have been fully considered. Examiners response is as follows:

2.1 Regarding the objection to Claim 17 regarding minor informalities:

The Examiner thanks the applicant for amending Claim 17 and hereby withdraws the earlier objections to that claim.

2.2 Regarding Applicant's response to the rejections of Claims 1, 28, 29, 33 and 60:

Applicant has argued:

> The Applicant's position is that, at least, and for reasons already stated in an Office Action response mailed June 16, 2003 (to which the Examiner is again referred):
>
> 1) with respect to independent claims 1, 28, and 33: the claim limitation "reducing a string to a pi model, the pi model having a pair of cross capacitors" is not taught or suggested by any combination of matter disclosed in Nakamura, Muddu and Dansky;
>
> 2) with respect to independent claims 29 and 60:
>
> the claims limitation "a pair of cross capacitors associated with a pi model, the pi model reduced from a string having more than a pair of cross capacitors" is not taught or suggested by any combination of matter disclosed in Nakamura, Muddu and Dansky;
>
> 3) with respect to independent claims 18 and 50:
>
> the claim limitation "a plurality of cross capacitors on a node, each of the cross capacitors corresponding to a different proximate trace" is not taught or suggested by any combination of matter disclosed in Nakamura, Muddu and Dansky.
>
> Therefore, at the core of the dispute between the Examiner and the Applicant is that any combination of matter disclosed in Nakamura, Muddu and Dansky fails to teach or suggest all of the Applicant's claim

> limitations. "To establish a prima facie case of obviousness ... the prior art reference (or references when combined) must teach or suggest all the claim limitations." MPEP 2143

The Examiner maintains that the *Nakamura* reference teaches a sting model and that it would be an obvious improvement for an artisan of ordinary skill to have used a a pi model reduced from a string in such a manner as argued in the previous office action.

> The Applicant respectfully submits that the Examiner has fallen short of the burden placed on the Examiner to show that all of the Applicant's claim elements are covered by the Nakamura, Muddu and Dansky references. The Examiner has only shown that a few key words can be found in the prior art; and, likewise, has failed to show that whole concepts communicated by the Applicant's independent claim language can be found in the prior art. As such, it appears that the Examiner has done nothing more that perform a keyword search and cobble up an Office Action without any understanding of the Applicant's independent claims or the teachings of the prior art.

The Examiner asserts that using a string as a method of modeling circuit characteristics is an obvious method of modeling and that an artisan of ordinary skill would find using a string model to measure circuit parasitic phenomena would be an obvious variation of the prior art of record.

> 1) **provide a clear explanation** where the claim limitation "reducing a string to a pi model, the pi model having a Pair of cross capacitors" can be found from the Nakamura, Muddu and Dansky references;

Here is the explanation, using strings for modeling characteristics of a circuit, which can have multiple paths is a known and easy to use method of modeling circuit characteristics as disclosed in the *Nakamura* reference. The use of a string model is efficient because of the need to model different pathways through complex circuit designs. Using *"pi"* models is VERY well known in the Engineering arts, every Electrical Engineering undergraduate program teaches *"pi"* models, the *Muddu* reference is only relied upon to provide clear evidence as required under the statute bar. Cross capacitors, used to model parasitic effects (or cross talk) in circuit traces that

are close to each other, is a phenomena that has been known in the Electrostatic Physical science area of knowledge since the time of Faraday, the *Dansky* reference was used to fulfill the statutory requirement, to provide evidence.

> 2) **provide a clear explanation** where the claim limitation "a pair of cross capacitors associated with a Pi model, the pi model reduced from a string having more than a pair of cross capacitors" can be found from the Nakamura, Muddu and Dansky references;

Please see the preceding explanation.

> 3) provide a clear explanation where the claim limitation "a plurality of cross capacitors on a node, each of the cross capacitors corresponding to a different proximate trace" can be found from the Nakamura, Muddu and Dansky references.

Please see the preceding explanation.

In the Office Action response mailed September 8, 2003 the Examiner has criticized the Applicant's comments in the Applicant's Office Action response mailed June 16, 2003. The Applicant respectfully submits that the Examiner's comments are off-point in a number of regards as elaborated on in more detail immediately below.

The Examiner would like to apologize to the Applicant if, in any way, the Examiner's comments have seemed to be unfairly critical. The Examiner is only trying to perform an Examination of Applicant's claim language, which is a reasonable interpretation of the limitations set forth. It is noted by the Examiner that the Applicant's have not invoked 35 U.S.C. 112, 6th paragraph, i.e. *means plus function language*, which would narrow and limit the claim language to the directed limitations as disclosed in Applicants specification. The Examiner asserts that, while Applicant's specification has been used as a guide, that the Examiner believes the current interpretations set forth in regards to Applicant's claimed limitations, are reasonable. It is further noted that given the teachings of the *Nakamura* reference that, in the opinion of the

Examiner, it is reasonable that using a string structure for modeling circuit parasitic characteristics would be within the knowledge and scope of an ordinary artisan.

> Firstly, the Examiner contends that the Applicant attempted to argue that the Nakamura reference is a non analogous art (See, Office Action mailed 9/8/03, Page3). The Applicant made no such statement. Consistent with the Applicant's assertion that the combination of Nakamura, Muddu and Dansky fails to cover all of the Applicant's independent claim elements, the Applicant's statement that Nakamura "is an irrelevant prior art reference" (See, Office Action response mailed 6/16/03, pg. 17) is directed to the fact that there exists nothing of significance taught by Nakamura that could be used to cover anything claimed by the Applicant. Specifically, each of the Applicant's independent claims incorporate appropriate limitations that reveal the string to be a lumped element model of a trace (i.e., regarding Claim 1: "said string having a collection of lumped elements including cross capacitors"; regarding Claim 18: "said string having a collection of lumped elements"; regarding Claim 28: "said string having a collection of lumped elements including cross capacitors"; regarding Claim 29: "a string having more than a pair of cross capacitors"; regarding Claim 33: "said string having a collection of lumped elements including cross capacitors"; regarding Claim 50: "said string having a collection of lumped elements"; regarding Claim 60: "a string having more than a pair of cross capacitors"). The Nakamura reference uses the term "string" to refer to the surface of a semiconductor element without consideration of passive elements such as resistances and capacitances. Therefore the term "string" of Nakamura fails to cover the term "string" found in the Applicant's claims.

The Examiner appreciates the Applicant acknowledging the *Nakamura* reference is a valid prior art reference and is analogous art. The Examiner asserts that there is respectful disagreement as to the meaning and the usage of the string term in applicant's claims. The Examiner asserts that modeling *"lumped"* elements is known in the art, as recited in the rejections and the prior art of record.

> The Examiner has chastised the Applicant for not explicitly claiming "features upon which the applicant relies (i.e., Capacitive Coupling)" (See, Office Action mailed 9/08/03, pg. 3). Here, the Examiner seems to have failed to realize that the phraseology "capacitive coupling between interconnect lines" that appeared in the Applicant's arguments in the Office Action response mailed June 16, 2003 were invoking the term "cross capacitor"; or, has refused to interpret the term "cross capacitor" in a manner that is consistent with that discussed from page 2, line 12 to page 3, line 7 of the Applicant's specification (See, Office Action mailed 9/08/03, pg. 3 - "[a][though claims are interpreted in light of the specification, limitations from the specification are not read into the claims"). If it is the later, the Applicant asserts that the issue with respect to

> the term "cross capacitors" is an issue devoted more to claim interpretation than to the incorporation of limitations into the claims. As such, the Applicant respectfully asks: what interpretation of the term "cross capacitor" is the Examiner using that is: a) inconsistent with that discussed from page 2, line 12 to page 3, line 7 of the Applicant's specification so as to allow the Examiner to dismiss the Applicant's arguments regarding the teachings of Muddu; yet, b) sufficient for the Examiner to use Dansky as a prior art reference against the term cross capacitors" as it appears in the Applicant's claims?

The Examiner respectfully assures the Applicant that no chastening was intended. The Examiner asserts that there has been a difference of opinion regarding the claim rejections and is attempting to clarify the Examiner's position in a respectful manner. Please accept the Examiner's apology for any tone in the actions what could be considered, chastening. The Examiner asserts that any *"cross-capacitance"* is the parasitic capacitance created between two signal transmission lines created by the their close proximity to each other and the dialectic (or insulating) effect cause by the air, or in the case of an integrated circuit, the silicon that lies between the two conductors. A *"cross-capacitor"* is a capacitor that provides a capacitive bridge or AC shunt connection between the two conductive transmission lines over which current is flowing.

> In contrast, the Examiner's position in the present application effectively ignores the limitation "based on combinations of references" (i.e., that all claim elements are covered is not in dispute) so as to effectively read "one cannot show non obviousness by attacking references individually where the rejection is based on 35 USC 103(a)". This is a preposterous statement of the law because it removes the burden on the Examiner to establish a prima facie case of obviousness by finding each and every claim element in the prior art. The Applicant is certainly free, as is the situation in the present application, to demonstrate non obviousness by "attacking" a reference because it does not teach or suggest that which the Examiner purports it to so teach or suggest. That is, when the dispute is whether or not one or more claim elements are actually covered by a prior art reference, the portion of In re *Keller* and In re *Merck & Co.* that has been cited by the Examiner does not apply.

The Examiner asserts that there is a difference of opinion between the Applicant and the Examiner in regards to the limitations being used as prior art. The Examiner asserts that the combination of the prior art of record teaches the applicant's claimed limitations. The Exmainer has found applicant's arguments to be unpersuasive and upholds the earlier 35 U.S.C. 103 rejections claims 1-63.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 1-3, 5-13, 15-20, 22-35, 37-45, 47-52 and 54-63** are rejected under 35 U.S.C. as being unpatentable over **Nakamura U.S. Patent 6,192,330** in view of **Muddu U.S. Patent 6,314,546** and in further view of **Dannsky et al. U.S. Patent 6,028,989.**

3.1 As regards independent **Claims 1, 18, 28, 29, 33, 50 and 60** the *Nakamura* reference discloses, a machine readable storage medium with at least one processor **(Figure 35**

Item 6, Col. 7 Lines 39-50), and a string model **(Figures 3, 5, 6, 9, 22A, 22B, 23, 24, 25, 26, 27, 28, 30A, 30B, 30C, 34).**

However, the *Nakamura* reference does not expressly disclose modeling a trace lumped elements, cross capacitors, a pi model and applied noise voltage.

The *Muddu* reference discloses modeling a trace **(Figure 1),** a pi model **(Figures 8b, 8c).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because *(motivation to combine)* when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, ***(Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50).***

The *Nakamura* reference does not expressly disclose lumped elements, cross capacitors and applied noise voltage.

The *Dannsky et al.* reference discloses lumped elements **(Col. 7 Lines 9-67, Col. 8 Lines 1-6)** cross capacitors **(Col. 7 Line 16),** and applied noise voltage **(Col. 1 Lines 15-18, Lines 63-67, Col. 2 Lines 1-17).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Dannsky et al.* reference because *(motivation to combine)* it is important to calculate in an efficient manner the voltage noise characteristics of an integrated circuit design ***(Dannsky et al. Col. 1 Lines 55-67, Col. 2 Lines 1-33).***

3.2 As regards the limitation disclosed in independent **Claim 28** regarding an apparatus, the *Nakamura* reference discloses **(Figure 35).**

3.3 As regards **Claims 2, 3, 5, 19, 20, 22, 23, 34, 35, 37, 51, 52 and 54** the *Nakamura* does not expressly disclose reducing the number of capacitors and resistors in the model and the O'Brien/Savarino method.

The *Muddu* reference discloses reducing the number of capacitors and resistors in the model and the O'Brien/Savarino method, **(Figure 4, Col. 5 Lines 35-67, Col. 6 Lines 1-67, Col. 7 Lines 1-2).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because *(motivation to combine)* when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, ***(Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50).***

3.4 As regards **Claims 6, 38 and 55** the *Nakamura* reference does not expressly disclose a "pi" model.

The *Muddu* reference discloses a "pi" model **(Figure 8b and 8c).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because *(motivation to combine)* when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, ***(Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50).***

3.5 As regards **Claims 7, 32, 39, 56 and 63** the *Nakamura* reference does not expressly disclose a voltage ramp.

The *Muddu* reference discloses a voltage ramp **(Figure 2b).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because *(motivation to combine)* when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, ***(Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50).***

3.6 As regards **Claims 8, 24 and 40** the *Nakamura* reference does not expressly disclose a ramp time and a driving transistor.

The *Muddu* reference discloses a ramp time and a driving transistor **(Figures 1, 2a, 2b, 3, 4, 5a, 5b, 6a, 6b, 7a, 7b, 8a, 8b, 8c, 8d and 8e, Col. 3 Lines 44-67, Col. 4 Lines 1-67, Col. 5 Lines 1-67, Col. 6 Lines 1-67, Col. 7 Lines 1-2).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because *(motivation to combine)* when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, ***(Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50).***

3.7 As regards **Claims 9 and 41** the *Nakamura* reference does disclose a string model, however it does not expressly disclose a pi model.

The *Muddu* reference discloses a pi model **(Figures 8b, 8c).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because *(motivation to combine)* when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, ***(Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50).***

3.8 As regards **Claims 10 and 42** the *Nakamura* reference does not expressly disclose a linear source.

The *Muddu* reference discloses a linear source model **(Figures 8a, 8c, Col. 8 Lines 8-14).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because *(motivation to combine)* when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, ***(Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50).***

3.9 As regards **Claims 11, 12, 43, 44 and 57** the *Nakamura* reference does not expressly disclose a victim node of the pi model.

The *Dansky et al.* reference discloses a victim node of the pi model **(Col. 1 Lines 24-26, Col. 3 Lines 15-16, Col. 3 Lines 40-48).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Dannsky et al.* reference because *(motivation to combine)* it is important to calculate in an efficient manner the voltage noise characteristics of an integrated circuit design ***(Dannsky et al. Col. 1 Lines 55-67, Col. 2 Lines 1-33).***

3.10 As regards **Claims 13, 26, 27, 58 and 59** the *Nakamura* reference does not expressly disclose a second noise voltage to the pi model.

The *Dansky et al.* reference discloses a second noise voltage applied to the pi model **(Col. 3 Lines 40-49).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Dannsky et al.* reference because *(motivation to combine)* it is important to calculate in an efficient manner the voltage noise characteristics of an integrated circuit design ***(Dannsky et al. Col. 1 Lines 55-67, Col. 2 Lines 1-33).***

3.11 As regards **Claims 15, 16 and 25** the *Nakamura* reference does not expressly disclose calculating the peak noise.

The *Dansky et al.* reference discloses calculating peak noise **(Col. 7 Lines 60-67, Col. 8 Lines 1-6).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Dannsky et al.* reference because *(motivation to combine)* it is important to calculate in an efficient manner the voltage noise characteristics of an integrated circuit design ***(Dannsky et al. Col. 1 Lines 55-67, Col. 2 Lines 1-33).***

3.12 As regards **Claims 17 and 49** the *Nakamura* reference does not expressly disclose resistors in series and capacitors in parallel reduced into a pi-model.

The *Muddu* reference discloses resistors in series **(Figure 5a, 5b, Col. 6 Lines 15-25)** and capacitors in parallel **(Figures 8b, 8c).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because *(motivation to combine)* when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, ***(Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50).***

3.13 As regards **Claims 30 and 61** the *Nakmura* reference does not expressly disclose discrete samples.

The *Mudda* reference discloses discrete load capacitances **(Col. 4 Lines 14-22).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because *(motivation to combine)* when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, ***(Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50).***

3.14 As regards **Claims 31, 45, 47, 48 and 62** the *Nakamura* reference does not expressly disclose applied noise voltage.

The *Dannsky et al.* reference discloses applied noise voltage **(Col. 1 Lines 15-18, Lines 63-67, Col. 2 Lines 1-17).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Dannsky et al.* reference because *(motivation to combine)* it is important to calculate in an efficient manner the voltage noise characteristics of an integrated circuit design ***(Dannsky et al. Col. 1 Lines 55-67, Col. 2 Lines 1-33).***

4. **Claims 4, 21, 36 and 53** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Nakamura U.S. Patent 6,192,330** in view of **Muddu U.S. Patent 6,314,546** and in further view of **Dannsky et al. U.S. Patent 6,028,989** and in further view of **"Modeling the Driving-Point Characteristics of Resistive Interconnect for Accurate Delay Estimation", Peter R. O'Brien and Thomas L. Savarino, IEEE 1989** hereafter referred as the **O'Brien and Savarino** reference.

4.1 As regards independent **Claims 1, 18, 33, 50** see the rejection in paragraph **3.1.**

4.2 As regards dependent **Claims 2, 3, 19, 20, 34, 35, 51 and 52** see the rejection in paragraph **3.3.**

4.3 As regards **Claims 4, 21, 36, 53** the *Nakamura* reference does not expressly disclose the Elmore influence reduction method.

The *O'Brien and Savarino* reference discloses the Elmore influence reduction method **(pages 513-514).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *O'Brien and Savarino* reference

because *(motivation to combine)* the methods disclosed in the *O'Brien and Savarino* reference provides greater accuracy in determining the voltage transfer ration between gates in an integrated circuit, ***(Abstact, Page 512 "Modeling the Driving-Point Characteristics of Resistive Interconnect for Accurate Delay Estimation", Peter R. O'Brien and Thomas L. Savarino, IEEE 1989).***

5. **Claims 14 and 46** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Nakamura U.S. Patent 6,192,330** in view of **Muddu U.S. Patent 6,314,546** and in further view of **Dannsky et al. U.S. Patent 6,028,989** and in further view of **Arsenault et al. U.S. Patent 6,396,256.**

5.1 As regards independent **Claims 1 and 33** see the rejection in paragraph **3.1.**

5.2 As regards dependent **Claims 13 and 45** see the rejection in paragraph **3.10 and 3.14** respecively.

5.3 As regards **Claims 14 and 46** the *Nakamura* reference does not expressly disclose voltage ramps having their ramp times in phase.

The *Arsenault et al.* reference discloses voltage ramps having their ramp times in phase **(Figures 2 and 3, Col. 1 Lines 45-55, Col. 2 Lines 48-63).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Arsenault et al.* reference because *(motivation to combine)* the *Arsenault et al.* reference discloses a method of detecting defects in a design before manufacturing and therefore remove the requirement to have to redesign a product after the initial investment in manufacturing has been made, ***(Arsenault et al. Col. 1 Lines 34-45).***

Conclusion

6. After reconsideration the Examiner has found applicant's arguments to be unpersuasive. Claims 1-63 are rejected.

6.1 This action is made **NON-FINAL** because of Applicants Request for Continued Examination (RCE) under 37 C.F.R. § 1.1114.

6.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 9:00 - 5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

DMC
January 25, 2004

HUGH JONES, Ph.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100